Abstracts

Via hole technology for microstrip transmission lines and passive elements on high resistivity silicon

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A process is described for the realization of via holes for microstrip transmission lines and passive elements on high resistivity silicon (/spl rho/>4000 /spl Omega/cm, 100 mm diameter, 100 /spl mu/m thickness). Via hole etching with vertical sidewalls is performed using an advanced silicon etch (ASE) process. The measured and simulated inductance of the gold metallized via hole is 22 pH. Measurements on a ring resonator-isolated by 550 nm thermal oxide from the substrate-yield a dielectric constant /spl epsiv//sub r/=11.2 and a loss tangent tan/spl delta/ around 10/sup -4/ for the 4000 /spl Omega/cm silicon substrate. Attenuation of microstrip transmission lines are <0.1 dB/mm at 20 GHz.

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